Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A process for manufacturing an integrated device, comprising:

forming integrated structures including semiconductor regions and isolation regions in a first wafer of semiconductor material;

forming interconnection structures of conductor material on a second wafer of semiconductor material, including forming plug elements, each including a base region and a bonding region, the bonding region of a metal material different from the base region and capable of reacting with said semiconductor regions of said first wafer; and

bonding said first wafer and said second wafer together, including causing said bonding regions to react with said semiconductor regions.

2. (Original) The process according to claim 1, wherein said semiconductor material is silicon, and said step of causing said bonding region to react comprises forming a metal silicide.

3. (Original) The process according to claim 1, wherein said metal material is chosen from among titanium, nickel, platinum, palladium, tungsten, and cobalt.

4. (Previously Presented) The process according to claim 1, wherein said plug elements have a height, and said step of forming integrated structures comprises forming an insulating material layer on top of the first wafer, said insulating material layer having a thickness smaller than said height of said plug elements, and forming openings in said insulating material layer to uncover selective portions of said wafer, and wherein said step of bonding said

first and second wafers comprises causing said bonding region to react with at least said selective portions of said wafer.

5. (Previously Presented) The process according to claim 1, wherein said step of forming integrated structures comprises forming an insulating material layer on top of the first wafer, and forming conductive regions of semiconductor material on top of said insulating material layer, and said step of bonding said first and second wafers comprises causing said bonding region to react with said conductive regions.

6. (Original) The process according to claim 1, wherein said step of forming interconnection structures comprises forming electrical connection regions of conductive material, and said step of forming plug elements comprises forming base regions of conductive material on top of and in direct electrical contact with said electrical connections regions, and forming said bonding regions on top of said base regions.

7. (Original) The process according to claim 1, wherein said step of forming integrated structures comprises forming integrated electronic components.

8. (Original) The process according to claim 1, wherein said step of forming integrated structures comprises forming micro-electromechanical systems.

9. (Original) The process according to claim 1, further comprising, before said step of bonding said first and second wafers, the step of forming self-alignment structures on said first and second wafers, and aligning said first and second wafers, using said self-alignment structures.

10. (Original) The process according to claim 9, wherein said step of forming self-alignment structures comprises forming at least one engagement seat in one of said first and

second wafers, and forming at least one engagement element on another of said first and second wafers in a position facing said engagement seat.

11. (Previously Presented) The process according to claim 10, wherein said step of forming integrated structures comprises forming an insulating material layer on top of the first wafer, said step of forming at least one engagement seat comprises forming a guide opening in said insulating material layer, said guide opening having a basically trapezium shape, with a major base and a minor base, and said engagement element having transverse dimensions smaller than said major base and greater than said minor base, and said step of aligning said first and second wafers comprises inserting said engagement element into said guide opening near said major base and displacing said second wafer with respect to said first wafer so to bring said engagement element towards said guide opening until said engagement element slots into said engagement seat.

12. (Original) The process according to claim 11, wherein said step of forming at least one engagement seat comprises forming a notch in said substrate beneath said guide opening, said step of forming an engagement element comprises forming at least one pin element of greater height than the thickness of said insulating material layer, and said step of displacing said second wafer comprises causing said pin element to snap into said notch before fittedly engaging said engagement element into said slotting seat.

13.-29. (Cancelled)

30. (Currently amended) A process for manufacturing an integrated device, comprising:

forming integrated structures in a first wafer of semiconductor material, the first wafer including an exposed semiconductor region;

forming, on a second wafer of semiconductor material, a plug element, including a base region and a bonding region, the bonding region being of a metal material ~~on a second wafer of semiconductor material~~; and

bonding the first and second wafers together by causing the bonding region of the plug element to react with the exposed semiconductor region.

31. (Previously Presented) The process of claim 1 wherein said metal material is palladium.

32. (Previously Presented) The process of claim 1, further comprising forming a through opening in the second wafer on a side of the wafer opposite the interconnection structures, such that a portion of an interconnection structure is exposed.

33. (Previously Presented) The process of claim 32, further comprising attaching a connection wire to the interconnection structure via the through opening.

34. (Previously Presented) A process for manufacturing an integrated device, comprising:

forming integrated structures in a first wafer of semiconductor material;

forming interconnection structures of conductor material on a second wafer of semiconductor material, including forming plug elements having a height, each having a bonding region of a metal material capable of reacting with said semiconductor material of said first wafer;

forming an insulating material layer on top of said first wafer of semiconductor material, said insulating material layer having a thickness smaller than said height of said plug elements;

forming openings in said insulating material layer to uncover selective portions of said first wafer; and

bonding said first wafer and said second wafer together, including causing said bonding regions to react with said selective portions of said wafer.

35. (Previously Presented) A process for manufacturing an integrated device, comprising:

forming integrated structures including semiconductor regions and isolation regions in a first wafer of semiconductor material;

forming interconnection structures of conductor material on a second wafer of semiconductor material, including forming plug elements, each having a bonding region of a metal material capable of reacting with said semiconductor regions of said first wafer;

forming a plurality of conductive regions on the second wafer;

forming connection regions connecting the conductive regions together;

forming one of the plug elements connected to one of the plurality of conductive regions; and

bonding said first wafer and said second wafer together, including causing said bonding regions to react with said semiconductor regions.

36. (Previously Presented) A process for manufacturing an integrated device, comprising:

forming integrated structures in a first wafer of semiconductor material, the first wafer having a face;

forming interconnection structures of conductor material on a face of a second wafer of semiconductor material, including forming plug elements each having a bonding region of a metal material capable of reacting with said semiconductor material of said first wafer;

forming self-alignment structures on the respective faces of said first and second wafers, and aligning said first and second wafers in a face-to-face configuration, using said self-alignment structures and

bonding said first wafer and said second wafer together, including causing said bonding regions to react with said semiconductor material of said first wafer.

37. (Previously Presented) A process for manufacturing an integrated device, comprising:

forming a structure in a first wafer of semiconductor material, including a movable component;

forming an integrated electronic component in a second wafer of semiconductor material;

forming a bonding layer, including a base region and a bonding region of a metal material on a selected one of the first or second wafer; and

bonding the first and second wafers together by causing the bonding region of the bonding layer to react with an exposed semiconductor material region on the one of the first or second wafers not selected.

38. (Previously Presented) A process for manufacturing an integrated device, comprising:

forming an integrated structure in a first wafer of semiconductor material;

forming a through connection region in a second wafer of semiconductor material;

forming a bonding layer, including a base region and a bonding region of a metal material on a selected one of the first or second wafer; and

bonding the first and second wafers together by causing the bonding region of the bonding layer to react with an exposed semiconductor material region on the one of the first or second wafers not selected.

39. (Previously Presented) The process of claim 38, further comprising forming an annular insulation region isolating the through connection region within the second wafer of semiconductor material.

40. (Previously Presented) The process of claim 38, further comprising:

forming a plurality of through connection regions, wherein the forming a through connection region step is comprised in the present step; and

forming a plurality of annular insulation regions, each isolating one of the plurality of through connection regions.